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GAZDZINSKI & ASSOCIATES
11440 WEST BERNARDO COURT, SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,241	LATTA, DAVID	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42* is/are allowed.

6)☒ Claim(s) *1-17,31-41 and 43-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 18, 2005 have been fully considered but they are not persuasive.

Applicant did not provide any arguments against the 35 USC 103(a) rejections of claims 1-17, 31-40, 44, or 45. However, Applicant amended claims 1, 7, 9, 31, 37-40, 44. The Examiner is not persuaded that these claims, as amended, overcome the prior art.

Therefore, the Examiner cannot allow claims 1-17, 31-40, 44, and 45.

2. Applicant's amendment to claim 46, filed January 18, 2005, with respect to the rejections of under 35 USC 103(a) as being unpatentable over Blackmon in view of Studor, and further in view of Gove, has been fully considered.

Although Applicant did not provide any arguments against this rejection, the Examiner is persuaded that Studor does not expressly disclose where user selections are used to generate hardware description language (HDL), as claimed. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground of rejection is made in view of Tensilica. Tensilica teaches the use of HDL as claimed.

Therefore, the Examiner cannot allow claim 46.

3. Applicant's arguments, see pages 13-15, filed January 18, 2005, with respect to the rejection of claims 41-43 as being unpatentable over Blackmon in view of Studor, and further in view of Gove, have been fully considered and are persuasive. The rejection of claims 41-43 has been withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 41 and 43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 41 recites the limitation "the instruction and operand decode mechanism" in line 15. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 43 recites the limitation "the instruction and operand decode mechanism" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of *True Application-Specific Embedded Processors Now a Reality for System-on-Chip Designs*, by Tensilica ("Tensilica").

With regard to claims 1, 9, 10, 31, and 44, Blackmon discloses a processor interface device (Fig. 1, item 8) and a method of accessing data disposed within a plurality of memory banks. The processor interface device includes at least one memory port (Fig. 2, items E and F), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 16a-16n), at least one function port (Fig. 2, items A, B, C, and D), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 10a-10d), a data transfer fabric (Fig. 1, item 14 and Fig. 2, item 30) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 2, items 32, 34, and 36) adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2-4, 14, 15, 32-34, and 45, Blackmon discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 14), and where the processor interface device further includes a macro function in data communication with the function ports (column 3, lines 48-50), the macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port. The processor interface device also further includes a plurality of macro functions (column 3, lines 48-50) in data communication with respective ones of the function ports, the interface device further adapted to allow simultaneous access to multiple

ones of the memory ports (column 3, lines 56-67 to column 4, lines 1-3) by respective ones of the macro functions via the function ports.

Blackmon does not expressly disclose where the processor interface device is used in an extensible processor. Regarding independent claim 1, Blackmon does not expressly disclose where the extensible processor includes a processor core, the configuration of which is determined based at least in part on the processor interface device. Regarding independent claims 9 and 31, Blackmon does not expressly disclose where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware.

Tensilica discloses an extensible processor (page 1, first paragraph). With regard to claim 1, Tensilica further discloses where the extensible processor includes a processor core (*see* "The Xtensa Solution and Design Flow" on page 5), the configuration of which is determined based at least in part on the processor interface device (pages 5-6). With regard to claims 9 and 31, Tensilica discloses where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware (*see* first paragraph under "The Xtensa Solution and Design Flow," on page 5).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Tensilica with the processor interface device of Blackmon. The suggestion or motivation for doing so would have

been to allow enable system designers to rapidly build highly differentiated and optimized synthesizable processor cores (page 1, first paragraph).

Therefore, it would have been obvious to combine Tensilica with Blackmon to obtain the invention as specified in claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45.

10. Claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of U.S. Patent No. 5,848,289 to Studor, et al. ("Studor").

With regard to claims 1, 9, 10, 25, 31, and 44, Blackmon discloses a processor interface device (Fig. 1, item 8) and a method of accessing data disposed within a plurality of memory banks. The processor interface device includes at least one memory port (Fig. 2, items E and F), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 16a-16n), at least one function port (Fig. 2, items A, B, C, and D), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 10a-10d), a data transfer fabric (Fig. 1, item 14 and Fig. 2, item 30) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 2, items 32, 34, and 36) adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2-4, 14, 15, 32-34, and 45, Blackmon discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 14), and where the processor interface device further includes a macro function in data communication with the function ports (column 3, lines 48-50), the

macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port. The processor interface device also further includes a plurality of macro functions (column 3, lines 48-50) in data communication with respective ones of the function ports, the interface device further adapted to allow simultaneous access to multiple ones of the memory ports (column 3, lines 56-67 to column 4, lines 1-3) by respective ones of the macro functions via the function ports.

Blackmon does not expressly disclose where the processor interface device is used in an extensible processor. Regarding independent claim 1, Blackmon does not expressly disclose where the extensible processor includes a processor core, the configuration of which is determined based at least in part on the processor interface device. Regarding independent claims 9 and 31, Blackmon does not expressly disclose where where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware.

Studor discloses an extensible processor (*see generally*, Fig. 2). With regard to claim 1, Studor further discloses where the extensible processor includes a processor core (Fig. 2, item 50), the configuration of which is determined based at least in part on the processor interface device (column 4, lines 18-51). With regard to claims 9 and 31, Tensilica discloses where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the

configuration of the first data processor being based at least in part on the selected extension hardware (column 4, lines 18-51).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Studor with the processor interface device of Blackmon. The suggestion or motivation for doing so would have been to allow a prior art CPU to be made extensible so that circuitry can be easily added to the extensible processor in order to meet differing customer needs, both in the present and in the future. This significantly reduces the cost for individual customer flexibility (*see* column 2, lines 57-67 and column 3, lines 38-43).

Therefore, it would have been obvious to combine Studor with Blackmon to obtain the invention as specified in claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45.

11. Claims 1-3, 9, 10, 31, 32, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,125,429 to Goodwin in view of Tensilica.

With regard to claims 1, 9, 10, 31, and 44, Goodwin discloses a processor interface device (Fig. 1, item 10) including at least one memory port (not shown), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 30, 32, 34, and 36), at least one function port (not shown), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 20, 22, 24, and 26), a data transfer fabric (Fig. 1, item 12) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 1, 14)

adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2, 3, 32, and 45, Goodwin discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 12), and where the processor interface device further includes a macro function in data communication with the function ports, the macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port.

Goodwin does not expressly disclose where the processor interface is used in an extensible processor. Regarding independent claim 1, Goodwin does not expressly disclose where the extensible processor includes a processor core, the configuration of which is determined based at least in part on the processor interface device. Regarding independent claims 9 and 31, Goodwin does not expressly disclose where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware.

Tensilica discloses an extensible processor (page 1, first paragraph). With regard to claim 1, Tensilica further discloses where the extensible processor includes a processor core (*see* "The Xtensa Solution and Design Flow" on page 5), the configuration of which is determined based at least in part on the processor interface device (pages 5-6). With regard to claims 9 and 31, Tensilica discloses where at least a portion of the processing device includes extension hardware selected by the user at

time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware (*see* first paragraph under "The Xtensa Solution and Design Flow," on page 5).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Tensilica with the processor interface device of Blackmon. The suggestion or motivation for doing so would have been to allow enable system designers to rapidly build highly differentiated and optimized synthesizable processor cores (page 1, first paragraph).

Therefore, it would have been obvious to combine Tensilica with Goodwin to obtain the invention as specified in claims 1-3, 9, 10, 31, 32, 44, and 45.

12. Claims 1-3, 9, 10, 31, 32, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,125,429 to Goodwin in view of Studor.

With regard to claims 1, 9, 10, 31, and 44, Goodwin discloses a processor interface device (Fig. 1, item 10) including at least one memory port (not shown), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 30, 32, 34, and 36), at least one function port (not shown), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 20, 22, 24, and 26), a data transfer fabric (Fig. 1, item 12) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 1, 14) adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2, 3, 32, and 45, Goodwin discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 12), and where the processor interface device further includes a macro function in data communication with the function ports, the macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port.

Goodwin does not expressly disclose where the processor interface is used in an extensible processor. Regarding independent claim 1, Goodwin does not expressly disclose where the extensible processor includes a processor core, the configuration of which is determined based at least in part on the processor interface device. Regarding independent claims 9 and 31, Goodwin does not expressly disclose where where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware.

Studor discloses an extensible processor (*see generally*, Fig. 2). With regard to claim 1, Studor further discloses where the extensible processor includes a processor core (Fig. 2, item 50), the configuration of which is determined based at least in part on the processor interface device (column 4, lines 18-51). With regard to claims 9 and 31, Tensilica discloses where at least a portion of the processing device includes extension hardware selected by the user at time of design of the processing device, the configuration of the first data processor being based at least in part on the selected extension hardware (column 4, lines 18-51).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Studor with the processor interface device of Goodwin. The suggestion or motivation for doing so would have been to allow a prior art CPU to be made extensible so that circuitry can be easily added to the extensible processor in order to meet differing customer needs, both in the present and in the future. This significantly reduces the cost for individual customer flexibility (*see* column 2, lines 57-67 and column 3, lines 38-43).

Therefore, it would have been obvious to combine Studor with Goodwin to obtain the invention as specified in claims 1-3, 9, 10, 31, 32, 44, and 45.

13. Claims 5-8, 11-13, 16, 17, 35-37, 40, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Tensilica, as applied to claims 1 and 9, above, and further in view of Gove.

As described above, Blackmon in view of Tensilica teaches all the features of claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45. Blackmon in view of Tensilica also teaches the features of claims 37 and 40 that are identical to those features found in claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45. Regarding claim 46, Blackmon in view of Tensilica teaches where user selections relating to the extension instruction set made at the time of design are used to generate a hardware description language (HDL) (*see* Tensilica, page 6).

With regard 5, 7, 8, 35, and 36, Blackmon in view of Tensilica does not expressly disclose a processor interface device, where the at least one macro functions is

controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in a pipeline fashion.

Gove discloses a processor interface device, where the at least one macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in pipeline fashion (Fig. 1, item 12).

With regard to claims 6, 16, 37, 40, and 46, Blackmon in view of Tensilica does not expressly disclose the processor interface device where the parent processor is a RISC processor and where the second data processor is a digital signal processor.

Gove discloses a processor interface device where the parent processor is a RISC processor and the second data processor is a digital signal processor (column 14, lines 46-56).

With regard to claims 11-13, 17, 21, and 22, Blackmon in view of Tensilica does not expressly disclose the device where at least one function controller has a plurality of registers. Gove discloses the claimed features as described in column 12, lines 20-50).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the parent processor of Gove with the processing interface device used in an extensible processor of Blackmon in view of Tensilica. The suggestion or motivation for doing so would have been so that the main processor could assure an orderly flow of data (column 7, lines 35-38).

Therefore, it would have been obvious to combine Gove with Blackmon in view of Tensilica to obtain the invention as specified in claims 5-8, 11-13, 16, 17, 35-37, 40, and 46.

14. Claims 5-8, 11-13, 16, 17, 35-37, and 40, are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Studor, as applied to claims 1 and 9, above, and further in view of Gove.

As described above, Blackmon in view of Studor teaches all the features of claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45. Blackmon in view of Studor also teaches the features of claims 37 and 40 that are identical to those features found in claims 1-4, 9, 10, 14, 15, 31-34, 44, and 45.

With regard 5, 7, 8, 35, and 36, Blackmon in view of Studor does not expressly disclose a processor interface device, where the at least one macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in a pipeline fashion.

Gove discloses a processor interface device, where the at least one macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in pipeline fashion (Fig. 1, item 12).

With regard to claims 6, 16, 37, and 40, Blackmon in view of Studor does not expressly disclose the processor interface device where the parent processor is a RISC processor and where the second data processor is a digital signal processor.

Gove discloses a processor interface device where the parent processor is a RISC processor and the second data processor is a digital signal processor (column 14, lines 46-56).

With regard to claims 11-13, 17, 21, and 22, Blackmon in view of Studor does not expressly disclose the device where at least one function controller has a plurality of registers. Gove discloses the claimed features as described in column 12, lines 20-50).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the parent processor of Gove with the processing interface device used in an extensible processor of Blackmon in view of Studor. The suggestion or motivation for doing so would have been so that the main processor could assure an orderly flow of data (column 7, lines 35-38).

Therefore, it would have been obvious to combine Gove with Blackmon in view of Studor to obtain the invention as specified in claims 5-8, 11-13, 16, 17, 35-37, and 40.

15. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Tensilica, further in view of Gove, as applied to claim 37 above, and further in view of U.S. Patent No. 6,581,191 to Schubert, et al. ("Schubert").

With regard to claims 38 and 39, and as discussed above, Blackmon in view of Tensilica, further in view of Gove, discloses all the features of claim 37.

Blackmon in view of Tensilica, further in view of Gove does not expressly disclose a software wrapper associated with the DSP to translate at least some signals exchanged between said DSP core and the standardized interface; or where the

software wrapper includes an HDL wrapper, the HDL wrapper being configured, at least in part at the time.

Schubert discloses a software wrapper and where the software wrapper is an HDL wrapper (column 9, lines 15-21 and column 28, lines 39-43).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the software wrapper of Schubert with the processor interface used in an extensible processor of Blackmon in view of Tensilica, further in view of Gove. The suggestion or motivation for doing so would have been to support regression testing of the instrumented design using functional simulation (column 28, lines 39-43).

Therefore, it would have been obvious to combine Schuber with Blackmon in view of Tensilica, further in view of Gove to obtain the invention as specified in claims 38 and 39.

16. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Studor, further in view of Gove, as applied to claim 37 above, and further in view of U.S. Patent No. 6,581,191 to Schubert, et al. ("Schubert").

With regard to claims 38 and 39, and as discussed above, Blackmon in view of Studor, further in view of Gove, discloses all the features of claim 37.

Blackmon in view of Studor, further in view of Gove does not expressly disclose a software wrapper associated with the DSP to translate at least some signals exchanged between said DSP core and the standardized interface; or where the software wrapper

includes an HDL wrapper, the HDL wrapper being configured, at least in part at the time.

Schubert discloses a software wrapper and where the software wrapper is an HDL wrapper (column 9, lines 15-21 and column 28, lines 39-43).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the software wrapper of Schubert with the processor interface used in an extensible processor of Blackmon in view of Studor, further in view of Gove. The suggestion or motivation for doing so would have been to support regression testing of the instrumented design using functional simulation (column 28, lines 39-43).

Therefore, it would have been obvious to combine Schuber with Blackmon in view of Studor, further in view of Gove to obtain the invention as specified in claims 38 and 39.

Allowable Subject Matter

17. Claim 42 is allowed.

18. Claims 41 and 43 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

19. The following is a statement of reasons for the indication of allowable subject matter:

a. The primary reason for the allowance of claim 42 is the inclusion of the limitation "wherein said processor core comprises a configuration determined at least in part based on user selections, said selections causing a prototype core

description to be modified in order to produce said configuration." The prior art is not directed to a processor device, as claimed, where the processor core includes a configuration based on user selections, which cause a prototype core description to be modified in order to produce the configuration.

b. The primary reason for the allowability of claims 41 and 43 is the inclusion of the limitation, "wherein said DSP core is specifically configured by said user to inter-operate with said at least one of (i) the instruction and operand decode mechanisms (ii) auxiliary registers and (iii) on-core memory resources of said RISC processor", as recited in claim 41, and the limitation "wherein said second processor core is specifically configured by said user at time of design to inter-operate with the instruction and operand decode mechanism, auxiliary register, and on-core memory resources of said first processor core" as recited in claim 43. The prior art is not directed to a processor device, as claimed, where a user configures a DSP to inter-operate with specific features of a second processor.

Conclusion

20. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DKM